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Levels 0 through 6, in addition to some hybrid systems, are introduced. This section contains some mathematically challenging concepts and should probably not be left for the student to read on his or her own. An instructor could also lecture over sections 7.4 Magnetic Disk Technology, 7.5 Optical Disks, and 7.6 Magnetic Tape. However, these sections are easily read by the student. However, if a teacher wants the students to have a mastery of all topics in Chapter 7, 6 lecture hours are more

reasonable. Going over several examples perhaps looking ahead to Chapter 10 can help motivate the study of this law. Some of the RAID levels are theoretical and have not been deployed, and this should be pointed out in lecture. While covering these levels, the advantages and disadvantages of each should be covered, in addition to situations in which one level is better or worse than another. She tells you that her new system runs at 1GHz, which makes it over three times faster than her old 300 MHz system. What would you tell her? You would explain Amdahl's Law. The processor is only one component contributing to the overall performance of a system. That is, what price would be charged for both upgrades to make their cost and performance improvement equal? Alternative good answer a. The CPU could save all information from the interrupt service routine that it was working on, just as if it were a user program. b. Could be a problem. c. Information coming from multiple sources at the same time could get garbled. Instruction-level pipelining is introduced as well. Realworld ISAs including Intel, MIPS, and Java are discussed to reinforce the concepts presented in the chapter. This chapter should be covered after Chapter 4. Lectures should focus on the following points: Instruction formats. Important issues here include instruction length, little versus big endian, register usage and the use of stacks, and expanding opcodes. Addressing.

Although addressing is an instruction design issue, there are many aspects to consider, the most important of which is addressing modes. Instruction-level pipelining. The fetch-decode-execute cycle can be overlapped, resulting in faster execution time. Resource conflicts, conditional branching, and data dependencies can slow this process down. Realworld examples of ISAs. Intel, MIPS, and the Java virtual machine are all presented to reinforce the concepts of the chapter. Required Lecture Time The important concepts in Chapter 5 can typically be covered in 3 lecture hours. However, if a teacher wants the students to have a mastery of all topics in Chapter 5, 8 lecture hours are more reasonable. If lecture time is limited, we suggest that the focus be on instruction formats including big versus little endian, use of registers, and instruction length and addressing with considerable attention paid to the various modes. Page 1 Many students comprehend the concept, but don't see the significance. The various software applications listed in this chapter will help the instructor make this point. Students often have difficulty understanding stack machines. It is important to emphasize that not ALL instructions on stack machine have zero operands, but rather, the instructions that allow for operands are limited. The concept of expanding opcodes is sometimes difficult for students as well. We suggest going over a small example in detail. When covering the addressing modes, we suggest that instructors include many examples, as this is one concept that tends to be easier to understand through examples. Students often confuse instruction-level pipelining with other types of pipelining. It is important to stress that there are many types of pipelining, but in this chapter only pipelining the fetch-decode-execute cycle is addressed.

Although the real-life examples can be left for students to read, these case studies provide the instructor with a means to tie the concepts from this chapter together, as well as a method for motivating study of the concepts from this chapter. Answers to Exercises 1. Assume you have a machine that uses 32-bit integers and you are storing the hex value 1234 at address 0. a. Show how this is stored on a big endian machine. b. Show how this is stored on a little endian machine. c. If you wanted to increase the hex value to, which byte assignment would be more efficient, big or little endian. Explain your answer. a and b. Address Big Endian Little Endian c. Little endian is more efficient because the additional information simply needs to be appended. Assume each value starts at address Draw a diagram of memory for each, placing the appropriate values in the correct and labeled memory locations. Page 2. For example, the value from Problem 3, sent as the value 511 on a big endian machine, would be read as the value 510 on a little endian machine. 5. The Population Studies Institute monitors the population of the United States. In 2000, this institute wrote a program to create files of the numbers representing the various states, as well as the total population of the U.S. This program, which runs on a Motorola Page 3 The Institute runs the program and then ships the output files to state agencies so the data values can be used as input

into various applications. However, one Pennsylvania agency, running all Intel machines, encountered difficulties, as indicated by the following problem. When the 32bit unsigned integer 1D2F37E8 16 representing the overall U.S. population predication for 2003 is used as input, and the agencys program simply outputs this input value, the U.S. population forecast for 2003 is far too large. Can you help this Pennsylvania agency by explaining what might be going wrong. Hint They are run on different processors.

Intel and Motorola use different endianness. If the program on the Intel machine does not adjust for this, then the integer is interpreted incorrectly. 6. There are reasons for machine designers to want all instructions to be the same length. Why is this not a good idea on a stack machine. The only instructions on a stack machine that need to address memory are push and pop. So an operand field is required, which implies the instruction field must be divided into an opcode and an operand. However, the other instructions need not access memory and can thus consist of only the opcode. Suppose there are address instructions. How many 1address instructions can be formulated. Explain your answer. There are address instructions. There are only a total of address instructions allowed if we have 32bit instructions two addresses take up 24 bits, leaving only 8 bits for the opcode. Looking at the 8 bit opcode, assume bit patterns 0 through 249 are used for the 250 twoaddress instructions. Then there are 6 bit patterns left for one address instructions. Remember the rules of precedence for arithmetic operators. Is it possible to have 5 2address instructions 45 1address instructions Page 5 Justify your answer. b. Assume that a computer architect has already designed 6 twoaddress and 24 zeroaddress instructions using the instruction format above. What is the maximum number of oneaddress instructions that can be added to the instruction set a. Yes. The 2address instructions could be represented 000xxxxxxx through 100xxxxxxx using 000 through 100 for opcodes. The 1address instructions could use through 16, through 16, and through 13 more, for a total of 45. The 0address instructions could use through 16, and through 16. So we have 000 xxxx xxxx 100 xxxx xxxx xxxx xxxx xxxx xxxx xxxx address instructions address instructions address instructions 16 b. Assume the twoaddress instructions use bit patterns 000 xxxx xxxx through 101 xxxx xxxx.

Assume also that the zeroaddress instructions are of the format through 8, through 8, and through 8 These constitute the last 16 binary numbers possible with 11 bits. Then all instructions beginning with 110 xxxx through xxxx could be one address instructions 16. In addition, xxxx through xxxx could be one address instructions, giving us 14 more, for a total of address instructions. 12. What is the difference between using direct and indirect addressing. Give an example. Direct addressing provides the actual memory address of the operand in the instruction, whereas indirect addressing provides, as part of the instruction, a pointer to a memory location. For example, the instruction Load X interpreted using direct addressing would go to memory location X and load the value found there. Using indirect addressing, memory location X would be used as the effective address of what should actually be loaded. So if a value of 200 were found at location X, the value located at address 200 would be loaded. Page 6 Given memory and register R1 contain the values below R1 200 Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below Page 7 A nonpipelined system takes 200ns to process a task. The same task can be processed in a 5segment pipeline with a clock cycle of 40ns. Determine the speedup ratio of the pipeline for 200 tasks. What is the maximum speedup that could be achieved with the pipeline unit over the nonpipelined unit. The same task can be processed in a 5segment pipeline with a clock cycle of 20ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the theoretical speedup that could be achieved with the pipeline system over a nonpipelined system. In accordance with programming language practice, computing the expression should not change the values of its operands.

Add R1, B, C Add R2, D, E Load R1, B Add R1, C Load B Add C Push B Push C Mult A, R1, R2 Load R2, E Store Temp Add 3address machine Add R2, E Load D Push D Mult R2, R1 Add E Push E Store

A, R2 Mult Temp Add 2address machine Store A Mult Store A 1address machine 0address machine 18. A digital computer has a memory unit with 24 bits per word. The instruction set consists of 150 different operations. All instructions have an operation code part opcode and an Page 8 The computer has an instruction format with 4 fields an opcode field; a mode field to specify 1 of 7 addressing modes; a register address field to specify one of 60 registers; and a memory address field. Assume an instruction is 32 bits long. Suppose an instruction takes four cycles to execute in a nonpipelined CPU one cycle to fetch the instruction, one cycle to decode the instruction, one cycle to perform the ALU operation, and one cycle to store the result. In a CPU with a 4stage pipeline, that instruction still takes four cycles to execute, so how can we say the pipeline speeds up the execution of the program. For one instruction, there is no speedup. The speedup comes with the parallel execution of multiple instructions. While the first instruction is decoding, the second can be fetched; while the first instruction is performing the ALU instruction, the second can be decoding, and the third can be fetched, etc. 21. Pick an architecture other than those covered in this chapter. Do research to find out how your architecture approaches the concepts introduced in this chapter, as was done for Intel, MIPS, and Java. No answer given. Page 9 Given memory as follows Memory What would be loaded into the AC if the addressing mode for the operand is a. immediate b. direct c. indirect a. 800 b. 900 c Write the following expression in postfix reverse Polish notation. The same task can be processed in a 5segment pipeline with a clock cycle of 60ns. The instruction set consists of 128 different operations.

All instructions have an operation code part opcode and an address part allowing for only one address.Computer Systems Design and Architecture 2.1, 2.2, 3.2 These computers are designed and constructed based on digital and Integrated Circuit Dr. HASAN HUSEYIN BALIK DECEMBER The concept of addressing data in computations. The implications for our machine designs Architecture Vocabulary Let s review a few relevant hardware definitions In general, a VM Virtual Machine is a hypothetical machine implemented in either hardware or software that directly Please review the entire quiz first and then budget your time carefully.ISA provides the level of abstraction between the software and the hardware One of the most important abstraction in CS It s narrow, Accumulatorbased machines A single register, called the accumulator, stores the operand before the operation, and stores the result after the operation.Calculate the speedup of Basic Control Signals. Basic Control Signals Arbitrary pick Motorola Digital VAX Divide algorithm. DIVIDE HARDWARE Version 1 We will see that the stack ADT and its implementation are very simple. If so, show an example; if not, prove Schematic Diagram of a Computer. The CPU. The Bus. Main Memory. It is a multipurpose, programmable EEC180B Lab 7 MISP Processor Design Spring 1995 John Magee 30 July 2013 Some material copyright Jones and Bartlett.In this introduction, each component of the machine is briefly described. This The Z80 microprocessor needs an We ll make many comparisons between the MIPS and 8086 To achieve Specifically, a stack is a dynamic set of elements in which Logic pin out of 8085 microprocessor Address bus unidirectional bus, used as high order bus Data bus bidirectional As its name implies It is an ordered collection of items into which JinFu Li Department of Electrical Engineering National Central University Jungli, Taiwan Modern processors. Examples. Simplified architecture model.

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